Quantum Capacitance Limited Vertical Scaling of Graphene Field-Effect Transistor

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ABSTRACT A high-quality Y_2O_3 dielectric layer has been grown directly on graphene and used to fabricated top-gate graphene field-effect transistors (FETs), and the thickness of the dielectric layer has been reduced continuously down to 3.9 nm with an equivalent oxide thickness (EOT) of 1.5 nm and excellent insulativity. By measuring CV characteristics of two graphene FETs with different gate oxide thicknesses, the oxide capacitance and quantum capacitance are retrieved directly from the experimental CV data without introducing any additional fitting process and parameters, yielding a relative dielectric constant of $\kappa = 10$ for Y_2O_3 on graphene and an oxide capacitance of about 2.28 μF/cm^2. It is found that for a rather large gate voltage range, this oxide capacitance is comparable and sometimes even larger than the quantum capacitance of graphene. Since the total gate capacitance is determined by the smaller of the oxide and quantum capacitance, our results show that not much further improvement can be gained *via* further vertical scaling down of the gate oxide, suggesting that Y_2O_3 may be the ultimate dielectric material for graphene. It is also shown that the Y_2O_3 gate dielectric layer with EOT of 1.5 nm may also satisfy the ultimate lateral scaling requirement on the gate length of graphene FET and be used effectively to control a graphene FET with a gate length as small as 1 nm.

KEYWORDS: graphene field-effect transistor · quantum capacitance · yttrium oxide · gate dielectric · vertical scaling

Graphene has extremely high intrinsic carrier mobility and ultralong mean free length[1−4] and has therefore been considered as one of the most promising candidates to replace the silicon channel in metal−oxide−semiconductor (MOS) field-effect transistors (FETs) with superior performance to extend Moore's Law in future nanoelectronics.[4,5] Since FET is a capacitance-operated device in which the conductance between source and drain is modulated by the gate, the gate insulator is among of the most crucial elements determining the performance of the FET device. To maintain sufficient gate control on the conduction channel during the lateral dimension scaling down in order to improve performance and integrated density of integrated circuits (ICs), the distance between the gate and channel will be simultaneously scaled down; that is, a thinner and thinner gate oxide is required to improve the drain−current response of the transistor to the applied gate voltage and to avoid short channel effect.[6] Unfortunately, similar to other two-dimensional (2D) electron gas FET system,[7] the vertical scaling down in the graphene FET cannot be continued forever and the total gate capacitance in a FET device with a very thin gate oxide is ultimately limited by the current leakage *via* gate and quantum capacitance originated from the finite density of states of the channel and the extra energy needed to pump electrons to states with higher energy.[8,9] To explore the limit of vertical scaling of graphene FETs, an ultrathin insulator with very high-quality and large capacitance must be fabricated on top of graphene at first. Although there exist several methods for fabricating a high-quality and uniform insulating layer on graphene,[10−16] an extremely large gate capacitance that is comparable to quantum capacitance has not been achieved in solid-state graphene devices, and the vertical scaling behavior of graphene FETs down to their quantum limits has not been investigated.

From a fundamental point of view, accurate measurement of quantum capacitance of graphene also provides an important tool for exploring the density of state or electronic compressibility of the material. Recently, quantum capacitance of graphene was measured and then retrieved by several groups in solid-state graphene devices,[17−19] but only few accurate results were obtained that can be compared directly to theory. This is because in most cases a high-quality insulator layer cannot be grown readily on pristine graphene. To solve this problem, some functionalization or buffering layers were introduced before growing a high-k dielectric layer on graphene.[10−14] The additional buffer layers, however, would significantly reduce the total oxide capacitance, which is usually

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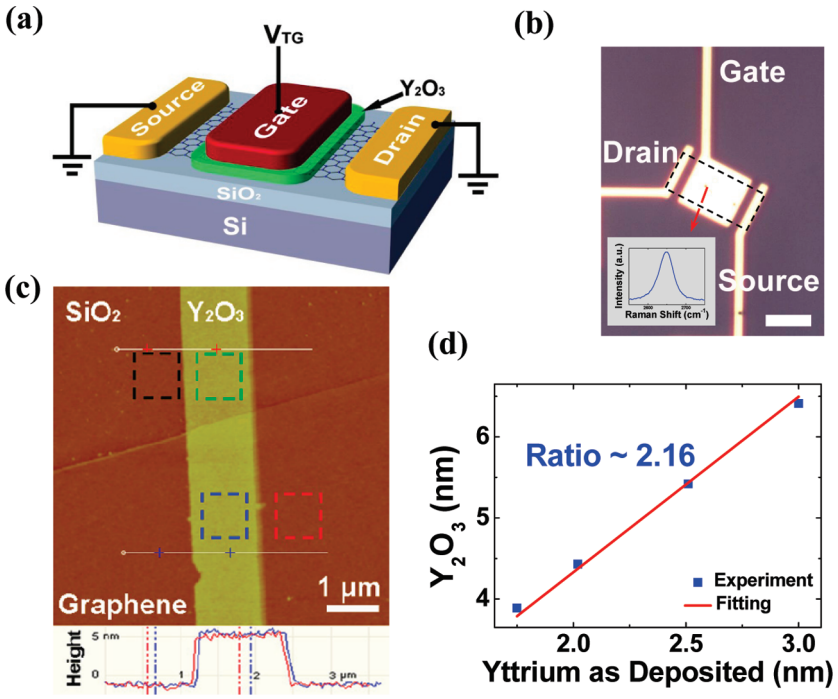

Figure 1. Single-layer graphene FET integrated with Y_2O_3 top-gate dielectric. (a) Schematics of the graphene device and experiment setup, where the graphene−Y_2O_3−Ti/Au capacitor stack lies on a SiO_2/Si substrate. (b) Typical optical image showing the as-fabricated graphene FET device. The graphene sheet is marked by the dashed frame, and the channel area covered by the top gate is $W = 4.5$ μm and $L = 7$ μm. The separation between source/drain electrodes to the top-gate electrode is 1.2 μm. The scale bar denotes 5 μm. Inset: typical Raman spectrum (with an excitation laser with wavelength 633 nm) of the graphene sample used in our device, suggesting the sample is a single-layer graphene. (c) Top: AFM topographic images showing an Y_2O_3 film on SiO_2 and single-layer graphene. The surface roughness values (σ) of SiO_2 (marked by dashed black square), Y_2O_3 on SiO_2 (marked by dashed green square), graphene on SiO_2 (marked by dashed red square), and Y_2O_3 on graphene (marked by blue square) are 230, 308, 238, and 295 pm, respectively. The scale bar of the topographic image is 1 μm. Bottom: the height profiles of the Y_2O_3 trips through the dashed lines, the red curve is on SiO_2 and the blue one is on graphene. (d) Thickness of the Y_2O_3 film (measured *via* AFM) as a function of the nominal thickness of the as-deposited Y film (measured directly using the crystal sensor in the deposition system).

far smaller than corresponding quantum capacitance, and as a result, the quantum capacitance cannot be accurately retrieved due to its very small contribution to the total gate capacitance. On the other hand, by using ionic liquid[20] as the gate insulator, the gate dielectric layer thickness can be reduced down to the subnanometer region where the quantum capacitance of graphene starts to dominate. However, an ion-rich environment introduces tremendous disturbances even at regions far from the Dirac point, and an unexpected strong asymmetric capacitance behavior was often observed.[20] Very recently, the capacitance and density of states of graphene were measured under varying electrical and magnetic field,[21] but the oxide capacitance is still much smaller than the quantum capacitance of the graphene.

In an earlier work, we reported that high-quality Y_2O_3 films can be uniformly grown on graphene *via* evaporating yttrium (Y) film followed by thermal oxidation.[22] In this article, we will demonstrate that the thickness of the Y_2O_3 film can be precisely controlled and shrunk continuously to improve the gate capacitance of the graphene FET. The oxide and quantum capacitances are retrieved directly from measured $C-V$ curves without introducing any additional fitting parameters, and the retrieved oxide capacitance from $C-V$ measurements is then compared with that by DC transport measurements. The obtained quantum capacitance of the graphene FET is found to typically account for more than 50% of the total gate capacitance and agrees excellently well with theory. In general, the gate capacitance improvement from vertical scaling down will become less effective and ultimately be limited by the quantum capacitance when the effective gate oxide layer thickness (EOT) is reduced to be less than a few nanometers. The thinnest Y_2O_3 film fabricated in this work has an EOT of 1.5 nm, which is shown to satisfy the requirement for efficient gate control for a graphene FET with a gate length down to 1 nm.

RESULTS AND DISCUSSION

We first consider the fabrication and characterization of the graphene FETs used for our following capacitance measurements. Figure 1a depicts the geometry of a top-gate graphene FET, and Figure 1b shows an optical microscope image of a real device. Atomic force microscopy (AFM) measurements (Figure 1c) show that the fabricated Y_2O_3 film is uniform over a large area and introduces hardly any additional roughness on graphene. The thickness of the Y_2O_3 film is

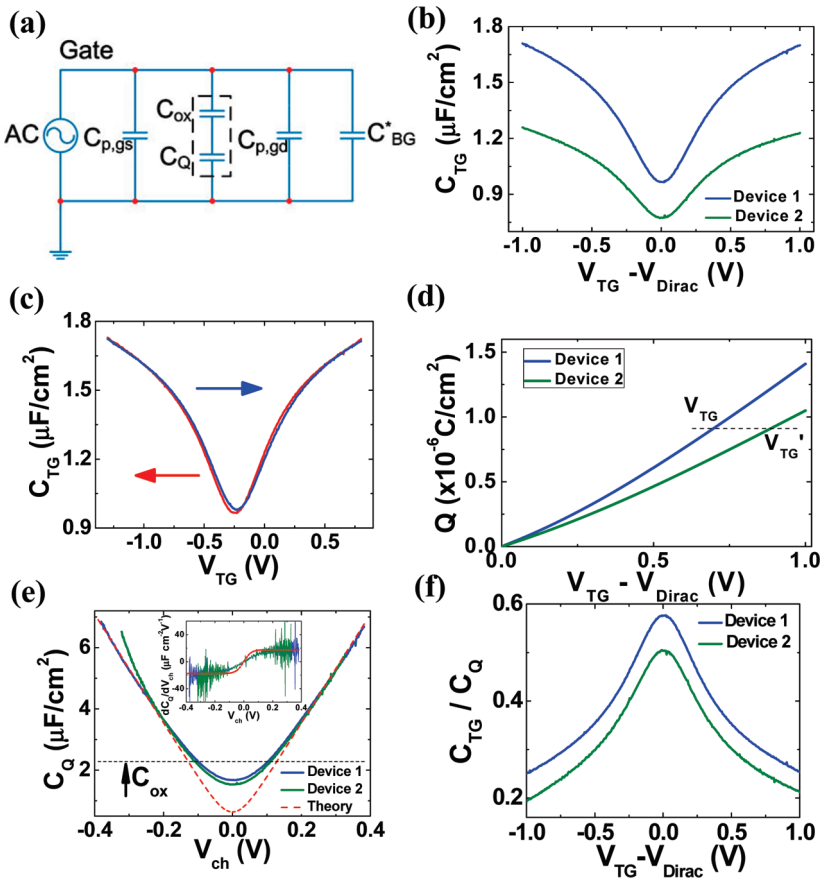

Figure 2. Measurement and retrieval of quantum capacitance of graphene FETs. (a) High-frequency equivalent circuit of a top-gate graphene FET for CV measurement. (b) Experimental total gate capacitances of graphene FETs with Y_2O_3 dielectric layer thicknesses of 3.9 nm (blue curve, device 1) and 5.6 nm (green curve, device 2), respectively. (c) Total gate capacitance curves measured by sweeping gate voltage from negative (positive) to positive (negative), showing little hysteresis behavior of the total gate capacitance in our graphene FETs with Y_2O_3 thickness of 3.9 nm. (d) V_{TG} dependent Q obtained for devices 1 and 2 by integrating the $C_{TG}-V_{TG}$ curves in panel b. (e) Theoretical and experimental quantum capacitance as a function of the channel voltage V_{ch}. The red dashed curve is the theoretical value for graphene at 300 K, with the Fermi velocity being 1.15 × 10^6 m/s. The horizontal dashed line is the oxide capacitance of device 1. Inset: experimental and calculated dC_Q/dV_{ch} as a function of V_{ch}. (f) Capacitance ratios between the total gate capacitance and quantum capacitance as a function of top-gate voltage.

linearly proportional to the as-deposited thickness of the evaporated Y film with a ratio of about 2.16 (Figure 1d). The total gate capacitance was measured between the gate electrode and the graphene channel beneath it with one electrode of the capacitor being the gate electrode and the other being the common terminal of source and drain. To guarantee the accuracy of the capacitance measurement, a graphene sheet larger than 50 μm^2 was used to fabricate the FET device. The area of the graphene beneath the top gate is thus large enough to ensure that the measured capacitance (typically larger than 200 fF in our devices) is larger than the measurement limit (typically smaller than 1 fF) of the instrument. In general, the measured capacitance C_M contains contributions from the top gate and other parasitic capacitances as shown in Figure 2a and can be modeled as

$$C_M = C_{TG} + C_{p,gs} + C_{p,gd} + C^*_{BG} \quad (1)$$

where C_{TG} is the total gate capacitance to be measured, $C_{p,gs}$ ($C_{p,gd}$) is the parasitic capacitance between the top-gate and source (drain) electrode, and C^*_{BG} is the parasitic capacitance originated from the back gate (but not the back-gate capacitance). The total contribution due to all parasitic capacitances was estimated by carrying out a measurement on a device with identical geometry but without the graphene channel beneath the top-gate dielectric. This contribution was found to be on the order of 1 fF and is negligible compared to the top-gate capacitance of our graphene devices, which is typically larger than 200 fF. To a good approximation, we may thus neglect the effect due to the parasitic capacitance to use $C_M \approx C_{TG}$.

The gate voltage dependent capacitances ($C_{TG}-V_{TG}$) for two typical graphene FETs (denoted as devices 1 and 2) with Y_2O_3 gate dielectric layer thicknesses of 3.9 and 5.6 nm, respectively, are shown in Figure 2b. Three distinct features are presented in these $C_{TG}-V_{TG}$ curves. (1) Almost perfect symmetry for electron and hole branches is observed centered at Dirac point, reflecting the symmetric band structure for electron and hole in graphene.[2,3] (2) The hysteresis is smaller

than 30 mV in the $C_{TG}-V_{TG}$ curve for different sweeping directions as shown in Figure 2c, suggesting that there exists few charge traps in the Y_2O_3 film or at the interface between Y_2O_3 and graphene. (3) The value of C_{TG} is seen to have increased by about 80% in changing the gate voltage from the Dirac point toward both positive (electron branch) and negative (hole) regions with a magnitude of ± 1 V. This tremendous change of C_{TG} may be attributed to the change of the quantum capacitance under varying gate potential. In principle, we can thus pick up ample information about the quantum capacitance of graphene from the $C_{TG}-V_{TG}$ curve.

The total gate capacitance can be modeled as a series of oxide capacitance and quantum capacitance (Figure 2a), that is

$$C_{TG}^{-1}(V_{TG}) = C_Q^{-1}(V_{ch}) + C_{OX}^{-1} \quad (2)$$

where C_{OX} is the oxide capacitance of the top gate, which is hardly dependent on V_{TG}, and C_Q is the quantum capacitance of graphene, which is dependent on V_{TG} *via* the graphene channel potential V_{ch}. The quantum capacitance can be extracted from the measured gate capacitance C_{TG} using eq 2 straightforwardly for any gate voltage V_{TG}:

$$C_Q(V_{ch}) = \frac{C_{OX}C_{TG}(V_{TG})}{C_{OX} - C_{TG}(V_{TG})} \quad (3)$$

where

$$V_{ch} = V_{TG} - \int_0^{V_{TG}} C_{TG}/C_{OX} dV_{TG}'$$

is the integral form of $C_{TG}dV_{TG} = C_{OX}d(V_{TG} - V_{ch})$, which results from charge conservation.

Since the growth of dielectric film on graphene is usually different from that on other substrates even with the same growth condition, the relative dielectric constant κ of the Y_2O_3 film on graphene may differ from that on silicon or other substrates. Since the directly measured C_{TG} includes inevitably the contribution of the quantum capacitance of graphene, the problem of retrieving κ value (or oxide capacitance) from *CV* measurements is not a trivial one. Two popular methods are widely used. The first is to fit experimental *CV* curves,[21] and the second is simply to use experiential value.[17−20] In this paper, we utilize the fact that in our experiments we can control the thickness of the Y_2O_3 film on graphene. We can therefore determine both the quantum capacitance of graphene and the relative dielectric constant of Y_2O_3 film simultaneously *via* measuring $C_{TG}-V_{TG}$ curves for two devices (Figure 2b) with different gate oxide thicknesses (for details see part I of Supporting Information).

We can eliminate the Q dependent C_Q far away from the Dirac point (for example with $|V_{ch}|$ larger than 0.2 V) and obtain the value of κ, which is about 10 here. Using this κ value, the oxide capacitances can be estimated to be 2.28 and 1.56 μF/cm^2, respectively, for the two devices with Y_2O_3 thicknesses of 3.9 and 5.6 nm. The V_{ch} dependent quantum capacitance C_Q can be retrieved by subtracting the oxide capacitance C_{OX} from the total gate capacitance C_{TG} by eq 3. The retrieved channel potential V_{ch} dependent C_Q values are shown in Figure 2e. It should be noted that the quantum capacitance near the Dirac point varies from sample to sample, which may be attributed to the different residue charges induced by charged impurities on graphene or in surroundings.[20,21,23−27]

The extracted C_Q from experimental measurements on two devices with different dielectric layer thicknesses has an ideal quantum capacitance which may be fitted using[9]

$$C_Q = \frac{2q^2kT}{\pi(\hbar v_F)^2} \ln\left[2\left(1 + \cosh\frac{qV_{ch}}{kT}\right)\right] \quad (4)$$

where the Fermi velocity v_F is found to be 1.15×10^6 m/s, which agrees excellently well with that reported by other groups.[21,28−31] It is obvious that the experimental C_Q results are well in agreement with theory except for these points near the Dirac point (Figure 2e). The quantum capacitance C_Q is seen to increase linearly with V_{ch} in regions far away from the Dirac point with a slope of 18 μF cm^{-2} V^{-1}, but the slope becomes much smaller and begins to deviate from theoretical value near the Dirac point, as shown in the inset of Figure 2e. Since the density of state at the Dirac point is dominated by electron−hole puddles induced by charged impurities around the graphene channel,[26,27,31,32] it is expected that the quantum capacitance should depart from theoretical values near the Dirac point, which is similar to that of the channel conductivity behavior near the Dirac point.

For an extremely thin gate dielectric layer, the quantum capacitance contributes not just a small correction to the total gate capacitance, instead it begins to dominate over the conventional oxide capacitance C_{OX}. We compared the larger C_{OX} (device 1) with retrieved V_{ch} dependent C_Q in Figure 2e, demonstrating clearly that for a large V_{ch} range (~0.2 V) C_{OX} is larger than C_Q. The contribution of the quantum capacitance to the total gate capacitance may be represented using the ratio C_{TG}/C_Q, and the resulting C_{TG}/C_Q-V_{TG} curve is shown in Figure 2f. This figure shows clearly that the contribution of quantum capacitance accounts for more than 20% of the total gate capacitance for the whole V_{TG} range from -1 to $+1$ V, and the contribution increases up to 58% at the Dirac point for device 1 and about 50% for device 2. For a V_{TG} range between -0.2 and 0.2 V, the ratio is always larger than 50%, showing that C_Q is dominating the total gate capacitance in our device 1.

While *CV* measurements can provide information on both oxide capacitance and quantum capacitance, the oxide capacitance C_{OX} can also be obtained by DC

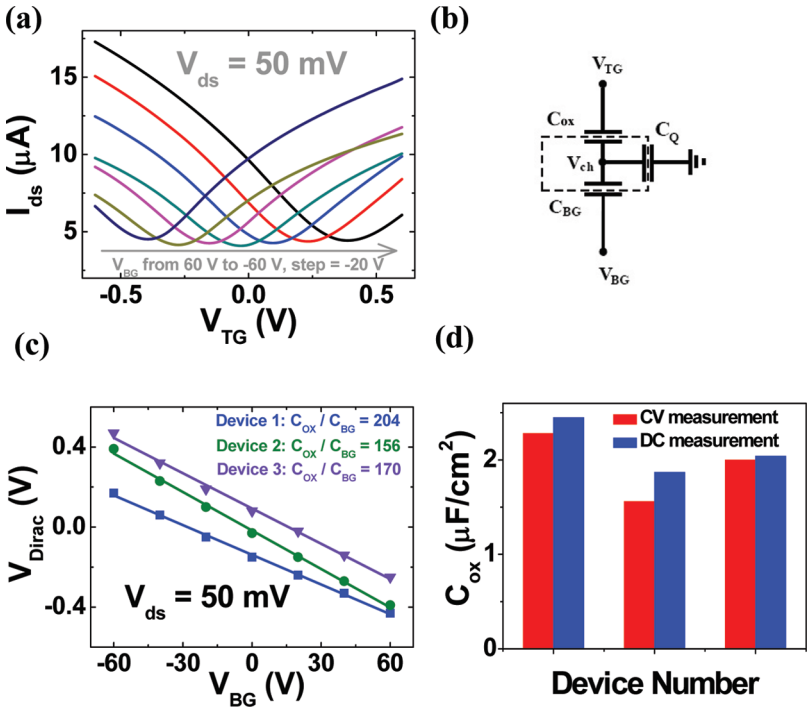

Figure 3. DC measurements and statistics on graphene FETs. (a) Typical gate transfer characteristics of a graphene FET, showing the shift of the Dirac point of the top-gate transfer characteristic at different back-gate voltage. (b) Equivalent capacitive circuit of a graphene FET that is being controlled by both the top gate and back gate simultaneously. (c) Top-gate voltage at the Dirac point as a function of the back-gate voltage. The triangles, circles, and squares are experiment data of three different devices, and solid lines are linear fittings of the experimental data. The inverse of the slope of the solid line gives the capacitance ratio C_{OX}/C_{BG}, where C_{BG} = 0.0121 μF/cm^2, being the capacitance of the back gate with a SiO_2 thickness of 287 nm. (d) Comparison of oxide capacitances retrieved from DC measurement and AC results for the three devices.

measurements.[11,15,16,33] Since the graphene channel may be simultaneously controlled by top gate and back gate, the Dirac point voltage $V_{TG,Dirac}$ in the top-gate transfer characteristic can be modulated by back-gate voltage V_{BG} (Figure 3a). Using the capacitive equivalent circuit scheme of the dual-gate graphene FET, as shown in Figure 3b,[34] it can be shown (see part II of Supporting Information) that the shift in the top-gate Dirac point voltage $\Delta V_{TG,Dirac}$ is linearly dependent on the change in the back-gate voltage ΔV_{BG} as

$$C_{OX}/C_{BG} = -\Delta V_{BG}/\Delta V_{TG,Dirac} \quad (5)$$

The shifts in the top-gate Dirac point $V_{TG,Dirac}$ as a function of back-gate voltage V_{BG} are shown in Figure 3c for three different graphene FETs and fitted using eq 5. From the slope of the fitted line, we can readily read out the ratio between the oxide capacitance of the back gate and top gate. Since the back-gate capacitance is known, the top-gate oxide capacitance can therefore be obtained without any prior knowledge on the quantum capacitance. The slope of the $V_{BG}-V_{TG,Dirac}$ curves (Figure 3c) reflects the top/back-gate ratio, that is, top-gate relative (to back-gate) efficiency, and for the three devices, we investigated the efficiencies of, respectively, 204, 156, and 170. It should be noted that these top-gate relative efficiencies are far beyond all of the previous published values.[11,12,15,16,33] Using the back-gate capacitance of 0.0121 μF/cm^2 (for a SiO_2 layer with a thickness of 287 nm and relative dielectric constant of 3.9, measured by ellipsometer), the top-gate capacitances of the three graphene FETs investigated are, respectively, 2.47, 1.89, and 2.06 μF/cm^2. We compared these oxide capacitances from DC transfer curves with those retrieved from *CV* measurements in Figure 3d, which shows good agreements of the results obtained through independent methods. The slight deviation may come from the imprecise estimation of the back-gate capacitance without considering the depletion layer capacitance of lightly doped silicon substrate or fluctuation in the thickness/relative dielectric constant in DC method, and in principle, the deviation is further magnified by top-gate efficiencies (about 200 times) when the top-gate oxide capacitances were calculated from these values. Carrier mobility is another key parameter for top-gated graphene FET with a high-k insulator. We can extract mobility for device 1 from the transfer curves shown in Figure 3a using a model described in ref 11 (see also Figure S1 and part III of Supporting Information). The retrieved electron and hole mobilities are, respectively, 1900 and 1800 cm^2/V·s. In principle, the carrier mobility of the top-gated graphene devices can be further improved through optimizing the quality of the Y_2O_3 film by improving oxidization temperature.

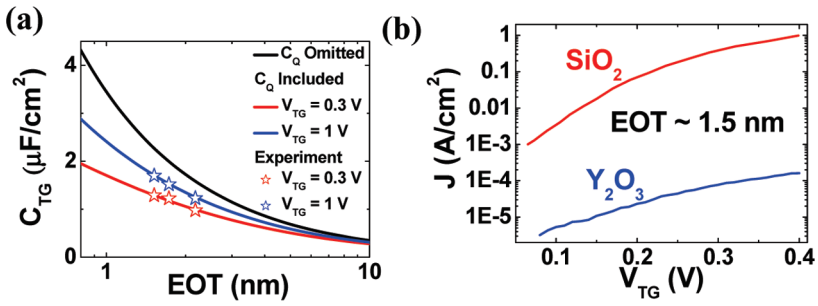

Figure 4. Vertical scaling behavior of graphene FETs. (a) Total gate capacitance with (dark blue for V_{TG} = 1 V and red for V_{TG} = 0.3 V) and without (black) the effect of quantum capacitance of graphene being taken into consideration. Solid curves denote theoretical calculations, and stars represent experiment results. (b) Gate leakage current density of a graphene FET with an Y_2O_3 layer thickness of 3.9 nm (corresponding to EOT ~ 1.5 nm) *vs* that of silicon MOS structure. The data of SiO_2 are adapted from Figure 2 of ref 35.

To estimate the limit performance or ultimate potential of graphene FETs, we now explore the vertical scaling behavior of the graphene FET where the quantum capacitance is expected to play an important role. The influence of the quantum capacitance on the total gate capacitance C_{TG} is shown in Figure 4a, and our measurements on three samples agree well with the theoretical predictions. It is clear that the improvement on C_{TG} *via* down scaling or reducing the gate dielectric layer thickness is becoming less effective with reducing equivalent oxide thickness (EOT) which is defined as

$$\text{EOT} = \frac{\varepsilon_{SiO_2}}{\kappa} t_{ox} \qquad (6)$$

where ε_{SiO_2} = 3.9 and κ = 10 are, respectively, the relative dielectric constants of the silicon oxide and Y_2O_3 on graphene. The smallest EOT realized in our graphene FETs is about 1.5 nm, which corresponds to the gate oxide EOT employed in the 45 nm silicon CMOS technology for low power circuits.[35] When V_{TG} = 1 V, where C_Q is relatively large, the total gate capacitance is reduced by $(C_{OX} - C_{TG})/C_{OX}$ = 26% as a result of quantum capacitance. This reduction becomes even more severe for smaller EOT or V_{TG}. When V_{TG} is reduced to 0.3 V, the reduction in the total capacitance is increased up to 44%. Therefore, the benefit of increasing the total gate capacitance *via* vertical scaling down will become less effective for thinner oxide owing to the limit imposed by the quantum capacitance of graphene.

It should be noted that EOT of 1.5 nm achieved here is the thinnest gate dielectric layer in all published graphene FETs. One important question that one would like to ask is how small a graphene FET could be given that we can now control the graphene channel *via* a top gate with an EOT of 1.5 nm. For a FET with planar channel geometry, such as a single-gated SOI MOSFET, the screening length λ is the key parameter for estimating the ultimate gate length and is given by[36,37]

$$\lambda = \sqrt{\frac{\varepsilon_{bulk} t_{bulk} t_{ox}}{\varepsilon_{ox}}} \qquad (7)$$

in which ε_{bulk} = 1[38] and t_{bulk} = 0.3 nm[39] are, respectively, relative dielectric constant and thickness of a single-layer graphene, and $\varepsilon_{ox} = \kappa = 10$ and $t_{ox} = 3.9$ nm are relative dielectric constant and thickness of Y_2O_3 gate insulator. Using these values in eq 7, we can then estimate the screening length to be about $\lambda = 0.34$ nm. Since the actual gate length should be approximately three times larger than λ,[36,37] the ultimate gate length of the graphene FET can thus be estimated to be about 1 nm for a gate dielectric layer with EOT of 1.5 nm. It is well-known that a FET device with a gate length of 1 nm must become invalid due to the tremendous direct tunneling current between source and drain; in reality, the gate length of graphene FET cannot be reduced down to 1 nm. We therefore conclude that an Y_2O_3 gate dielectric layer with EOT of 1.5 nm will be sufficient for graphene FETs with any reasonable scaled gate length, and in principle, it is not necessary to further improve the gate capacitance *via* reducing EOT.

In principle, the gate efficiency can still be improved by perhaps 10% *via* further reducing the gate dielectric layer thickness, but the price one has to pay is the increased leakage, which is another important parameter in oxide scaling. The gate leakage current density of our graphene FET is measured and shown in Figure 4b, showing clearly an approximately exponent dependence on gate voltage. The advantage of using high-κ dielectric material is amply demonstrated in Figure 4b. The leakage current curve through the Y_2O_3 gate dielectric layer with an EOT of 1.5 nm is found to be almost 3 orders of magnitude smaller than that through a thermally grown SiO_2 layer with the same EOT.[35,40]

CONCLUSIONS

In conclusion, the thickness of Y_2O_3 film has been shrunk continuously to improve the gate capacitance in graphene FET, and the thinnest EOT of about 1.5 nm with excellent insulativity has been integrated in graphene FET. The oxide capacitance and quantum capacitance are simultaneously retrieved from experimental *CV* curves without introducing any fitting parameters, and the retrieved oxide capacitances from

CV measurement are compared with that from DC transport measurements. Excellent agreement between the two results is found. Meanwhile, the quantum capacitance of graphene is precisely retrieved from total gate capacitance and found to agree perfectly with theory. It is shown that the gate capacitance improvement from vertical scaling down will become less effective, and the gate capacitance will be dominated by quantum capacitance when the thickness of the Y_2O_3 dielectric layer is reduced below 4 nm.

METHODS

Graphene was deposited by mechanical exfoliation of Kish graphite on silicon substrate, which was covered with a 287 nm thick SiO_2. The silicon substrate with high resistivity up to 18 kΩ·cm was used in order to reduce parasitic capacitance in AC measurement. Single-layer graphene samples were identified by optical contrast and Raman spectroscopy. To calculate the gate area precisely, the graphene was first tailored to a rectangle by electron beam lithography (EBL) and reactive ion etching (RIE). The gate was patterned by electron beam lithography, and then a thin uniform yttrium (Y) film was deposited by e-beam evaporation (EBE). The thickness of the Y film was detected by crystal oscillator sensor in the EBE system. The Y film was oxidized at 180 °C in air, and a uniform yttrium oxide film was then formed on graphene. An additional forming gas (Ar/H_2 = 5:1) annealing at 300 °C for 1 h in a furnace was carried out before source/drain and gate metal fabrication, so as to improve the dielectric quality of Y_2O_3 and reduce interface states between graphene and Y_2O_3. The accurate thickness and roughness of the final Y_2O_3 film on graphene were measured by atomic force microscope (AFM), as shown in Figure 1c. Source, drain, and gate electrodes were then formed through EBL, electron beam evaporation of Ti/Au film with a thickness of 5/45 nm, and followed by a standard lift-off process. All electrical measurements reported in this work were carried out by a probe station (Lakeshore TTP-4) in vacuum and at room temperature. DC transport measurements were carried out using a Keithley 4200 semiconductor analyzer and $C-V$ measurements by an Agilent 1500 B with a small AC modulation (30 mV and 50 kHz). Under $C-V$ measurements, the Si substrates were electrically separated from the chunk of probe station to reduce the substrate-relative parasitic capacitance.

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Supporting Information Available: Additional experimental details. This material is available free of charge *via* the Internet at http://pubs.acs.org.

NOTE ADDED AFTER ASAP PUBLICATION

This paper was published on February 16, 2011 with an error in the y-axis of Figure 4b. The corrected version was reposted on March 22, 2011.

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